

09711866

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<input type="checkbox"/>	L12	l11 and (test\$3) same (cell) with compar\$7 near2 (PARALLEL\$4 OR CONCUR\$7 OR SIMULTANES\$7 OR CONTEMPORan\$7 or CONTEMPO\$7 or contemporaneously) with (location or address)	5
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L12: Entry 3 of 5

File: USPT

Jan 27, 1987

DOCUMENT-IDENTIFIER: US 4639915 A

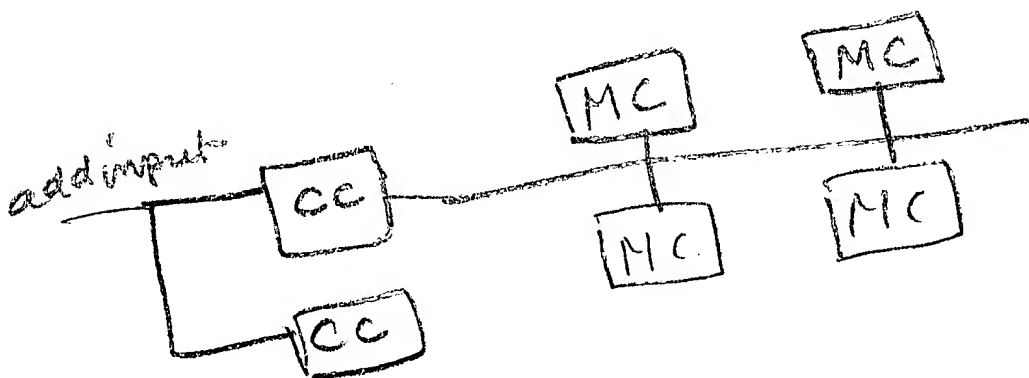
TITLE: High speed redundancy processor

Detailed Description Text (11):

The real time testing algorithm involves presenting the address coordinates of each faulty cell to catch buffer registers 32, 34, comparing the coordinates of that address with other information available thus far, and in some cases assigning a redundant row or column to the faulty cell. Such an assignment is called an auto-assignment. Upon making an auto-assignment the apparatus accepts one address coordinate of the faulty cell that will be thus repaired, into one of its fail registers 28, 30 and sets a corresponding status bit of catch buffer status circuits 55, 57, to indicate that the auto-assignment has been made.

Detailed Description Text (18):

After the real time testing has proceeded through a number of cells, several locations of the row catch buffer 32 may contain the X coordinate portion of addresses of faulty cells. These X coordinates are compared with incoming X coordinate data each time a new defective cell is discovered. The row catch buffer 32 includes logic circuits 49 (FIG. 7) for simultaneously comparing the contents stored in each of its locations with the address of a faulty cell that is coming in from the address lag register 46 on the conductors 42. Each location of the row catch buffer has its own independent compare circuit 49 and compare output circuit 53. (The compare outputs are independent from the address of the row/column pointer 40.) Whenever the contents of one of the row catch buffer locations matches the incoming fault address, the catch buffer 32 will produce a signal at its corresponding output line M0, M1, etc. of 53. For example, if the address at 42 matched the contents of the first and third row catch buffer locations of FIG. 7, M0 and M2 would produce an output signal.



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